

# New Frontier Process using Bio Technology (AOARD-114014)

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## **Background and Purpose:**

Large-scale integration (LSI) technology has been developed very rapidly to bring about the present information age. According to Moore's Law, four-fold improvements are achieved every three years, but even so, a higher speed, lower energy consumption and greater integration are increasingly required. In order to meet these requirements, nanoscale devices using quantum effects are being investigated very actively. However, conventional processes based on lithography technologies using light cannot produce these nanostructures. On the other hand, biotechnology has been recently making marked progress. It is known that many sophisticated functions of life are realized by the combination of nanometer-size biomolecules. In other words, cells are a collection of biomolecular machines and nanostructures that self-assemble. This leads to the idea that making use of self-assembling biomacromolecules is a reasonable approach for fabricating nanostructures.

## **Summary1: Three-Dimensional Nanodot-Type Floating Gate Memory Fabricated by Bio-layer-by-layer Method**

The properties of a nanodot-type floating gate memory with a multilayered nanodot array were investigated. High-density and uniform cobalt bio-nanodot (Co-BND) arrays were stacked on a SiO<sub>2</sub> tunnel oxide layer by a bio-layer-by-layer method (Bio-LBL). Memory properties, such as hysteresis width, charge retention, charging speed, and reliability, were improved by increasing the number of Co-BND arrays in a floating gate memory. This research confirmed that the proposed memory is promising for application in next-generation memory devices.

## **Summary 2. Guided Filament Formation in NiO-ReRAM by Embedding Gold Nanoparticle**

Resistive memory is a promising nanoscale device and has great potentials in nonvolatile memory. We demonstrate controllable positioning of conductive filament formation in NiO using gold nano particle (GNP). The 15 nm GNP was aligned on bottom electrode using biological process, bio nano process. Restricted nanoscale filament formation by the GNP has been observed by conductive atomic force microscopy (c-AFM) and the writing and erasing on defined area were achieved by nanometer scale. We further confirm that the forming

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voltage reduced by the GNP guided conductive filament formation. Cross-sectional transmission electron microscopy (TEM) determines that the lower forming voltage is due to the defects and grain boundaries in NiO layer formed by the GNP.

### Publication List:

- (1) Y.Ueoka, M.Fujii, H.Yamazaki, M.Horita, Y.Ishikawa, Y.Uraoka, “Analysis of Electron Traps in SiO<sub>2</sub>/IGZO Interface by Cyclic Capacitance–Voltage Method”, IEEE/ 2012 International Meeting for Future of Electron Devices, Kansai, p.58-59,2012.
- (2) H.Yamazaki, M.Fujii, Y.Ueoka, Y.ishikawa, M.Fujiwara, E.Takahashi, Y.Uraoka, “Highly Reliable a-InGaZnO Thin Film Transistors with New SiNx Gate Insulators”, IEEE/ 2012 International Meeting for Future of Electron Devices, Kansai, p.62-63, 2012.
- (3) Hiroki Kamitake, Kosuke Ohara, Mutsunori Uenuma, Bin Zheng, Yasuaki Ishikawa, Ichiro Yamashita, and Yukiharu Uraoka, “Nanodot-Type Floating Gate Memory with High-Density Nanodot Array Formed Utilizing Listeria Ferritin”, IEEE/ 2012 International Meeting for Future of Electron Devices, Kansai, p.50-51, 2012.
- (4) Shinji Araki, Min Zhang, Takahiro Doe, Li Lu, Masahiro Horita, Takashi Nishida, Yasuaki Ishikawa, and Yukiharu Uraoka, “Fabrication of Nano-Patterns Using Quick Gel-Nanoimprint Process”, IEEE/ 2012 International Meeting for Future of Electron Devices, Kansai, p.64-65, 2012.
- (5) Yana Mulyana, Masahiro Horita, Yasuaki Ishikawa, Yukiharu Uraoka, and Shinji Koh, “Characterization of Graphene Based Field Effect Transistors Using Nano Probing Microscopy”, IEEE/ 2012 International Meeting for Future of Electron Devices, Kansai, p.136-137, 2012.
- (6) Takahiro Doe, Shinji Araki, Masahiro Horita, Takashi Nishida, Yasuaki Ishikawa, and Yukiharu Uraoka, “Dependence of Semiconductor Nanoparticle Size on Spray Condition in Electro-Spray Deposition Method”, IEEE/ 2012 International Meeting for Future of Electron Devices, Kansai, p.60-61, 2012.
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- (8) Mutsunori Uenuma, Bin Zhen, Kentaro Kawano, Masohiro Horita, Yasuaki Ishikawa, Ichiro Yamashita and Yukiharu Uraoka, “Guided filament formation in NiO-resistive random access memory by embedding gold nanoparticles, Applied Physics Letters, 100, 083105 (2012).
- (9) Takashi Nishida, Kazushi Fuse, Mamoru Furuta, Yasuaki Ishikawa, and Yukiharu Uraoka, “Crystallization Using Biomineralized Nickel Nanodots of Amorphous Silicon Thick Films Deposited by Chemical Vapor Deposition, Sputtering and Electron Beam Evaporation”, Japanese Journal of Applied Physics, 51 (2012) 03CA01.

# New Frontier Process using Bio Technology (AOARD-114014)

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## 1. Three-Dimensional Nanodot-Type Floating Gate Memory Fabricated by Bio-layer-by-layer Method

A flash memory is used for various electrical devices, such as USB memory and SD cards, owing to its nonvolatility, high integration, and large capacity. In particular, a nanodot-type floating gate memory is promising for use as a future nonvolatile memory owing to the further scaling down of gate oxide, the reduction in operation voltage, and better writing and erasing operations. A nanodot array can be formed by various methods, such as thermal annealing and chemical vapor deposition (CVD). However, the size distribution and adsorption density of the nanodot array formed by these processes are not uniform.

Our research group has been investigating a semiconductor device process using protein which is a promising nanoelement for a semiconductor nanostructure fabrication process. Protein, which is produced on the basis of deoxyribonucleic acid (DNA) information, has significant features, such as nanometer size, structural uniformity, and self-assembly. Therefore, protein is one of the most attractive materials as a nanostructure-constructing component. Some types of protein can work as nanotemplates for synthesizing nanometer-size materials, such as nanowires and nanoparticles. This synthesis process is called biomineralization. The uniformity of

protein provides structural uniformity to biomineralized inorganic nanomaterials. The self-assembly ability of protein enables the obtained bioconjugate, protein, and inorganic material to form ordered nanostructures without any control from outside. Utilizing such merits, our research group proposed a nanodot-type floating gate memory with nanodot arrays formed by the protein ferritin.

Ferritin is a cage-shaped protein composed of 24 subunits that form a spherical supramolecular structure with a hollow cavity. The inner cavity and protein shell of ferritin are 7 and 12 nm, respectively. Ferritin can be used to construct various types of nanodot, such as Fe, Ni, and Co, within its cavity by biomineralization. The biomineralized nanodots are called bio-nanodots (BNDs). The BNDs constructed using ferritin are uniform in size and shape owing to the uniformity of ferritin.

However, even if the nanodots are packed as a two-dimensional array, the maximum adsorption density of a two-dimensional nanodot array formed using ferritin is limited to a value less than  $8.0 \times 10^{11} \text{ cm}^{-2}$ . It is also difficult to realize a nanodot array with a high adsorption density, such as more than  $10^{12} \text{ cm}^{-2}$ , which is exactly required for next-generation memory devices. Therefore, we proposed a nanodot-type floating gate memory with a multilayered nanodot array to increase the adsorption density of the nanodot array, as

shown in Fig. 1.1. The adsorption density of a nanodot array, as well as the amount of charge injected into the nanodot array, can be increased by stacking nanodot arrays. As a result, the performance and reliability of a nanodot-type floating gate memory can be significantly improved. We used a bio-layer-by-layer method (Bio-LBL) to stack nanodot arrays. Bio-LBL is a method of stacking ferritin arrays using titanium-binding ferritin (TBF). TBF has the abilities to be adsorbed onto specific materials (Ti, Ag, and Si) and to form  $\text{SiO}_2$  by biomineralization. A multilayered TBF array can be formed by repeating selective adsorption and biomineralization. In this study, we fabricated a nanodot-type floating gate memory with a multilayered nanodot array formed by Bio-LBL and measured the properties of the fabricated memory.

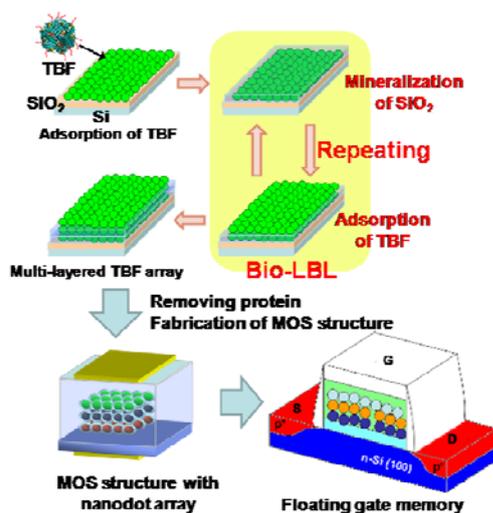


Fig. 1.1 Nanodot-type floating gate memory with multilayered nanodot array formed by Bio-LBL.

An ion-implanted p-Si (100) substrate was cleaned by the standard Radio

Corporation of America (RCA) cleaning method. After cleaning, a 3-nm-thick layer of  $\text{SiO}_2$  was formed as the tunnel oxide layer by rapid thermal annealing at  $900\text{ }^\circ\text{C}$  in  $\text{O}_2$  ambient. The surface of the  $\text{SiO}_2$  layer was cleaned and made hydrophilic by ultraviolet irradiation in an ozone atmosphere at  $115\text{ }^\circ\text{C}$  for 10 min. A solution of 0.5 mg/ml Co-accommodated TBF (Co-TBF) in 50 mM Tris-HCl (pH. 8.0) was dropped on the tunnel oxide layer, and the excess solution was removed by rinsing with Tris-HCl. After the adsorption of Co-TBF, the sample was dipped into a tetramethoxysilane solution, which was prehydrolyzed using 1 mM HCl to form an ultrathin  $\text{SiO}_2$  layer ( $\text{SiO}_2$  interlayer) on the surface of the Co-TBF array followed by Tris-HCl rinsing. Co-TBF arrays were stacked by repeating the adsorption of Co-TBF and biomineralization of  $\text{SiO}_2$ . After stacking Co-TBF by Bio-LBL, the outer shell of ferritin was removed by annealing in nitrogen ambient at  $500\text{ }^\circ\text{C}$  for 60 min, and a multilayered array of Co-BNDs acting as charge storage nodes was formed on the  $\text{SiO}_2$  tunnel oxide layer. A 20-nm-thick  $\text{SiO}_2$  layer was deposited at  $300\text{ }^\circ\text{C}$  by plasma-enhanced CVD (PECVD) as a control oxide layer covering the fabricated Co-BND array. After fabricating the MOS structure, the MOS structure was annealed in hydrogen ambient at  $650\text{ }^\circ\text{C}$  for 1 h to obtain a metal Co-BND array. Next, the sample was annealed in high-pressure  $\text{D}_2\text{O}$  ambient at 0.5 MPa and  $260\text{ }^\circ\text{C}$  for 1 h to improve the properties of the  $\text{SiO}_2$  gate oxide layer. Titanium was deposited as the gate electrode of the MOS devices. Finally, post-metallization annealing (PMA) was

performed in a reductive gas mixture (10% H<sub>2</sub> and 90% N<sub>2</sub>) at 450 °C for 1 h.

Figure 1.2 shows the cross-sectional transmission electron microscopy (TEM) image of the MOS capacitor with a multilayered Co-BND array. A black dotted circle indicates a Co-BND. Co-BND arrays were stacked by Bio-LBL, and each Co-BND was separated by a SiO<sub>2</sub> layer. The thickness of the SiO<sub>2</sub> layer formed by the biomineralization of TBF was about 1.5 nm. The ultrathin SiO<sub>2</sub> interlayer was formed by Bio-LBL.

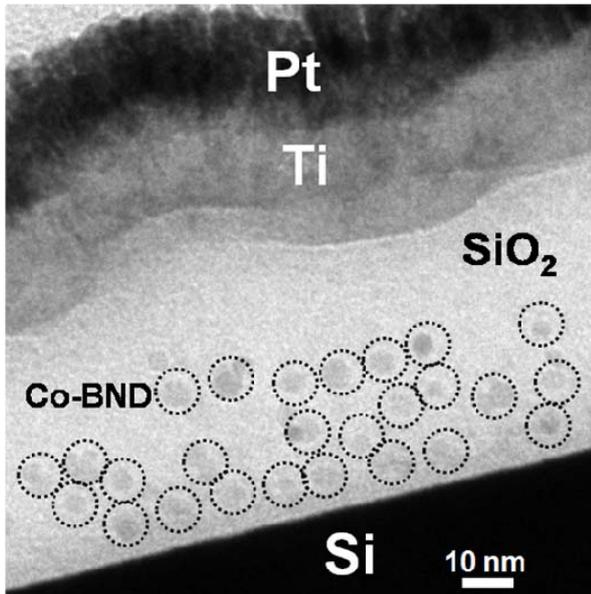


Fig. 1.2 Cross-sectional TEM image of memory.

Figure 1.3 shows the  $I_D$ - $V_G$  characteristics of the memory with a multilayered Co-BND array. The gate width and length were 2 and 0.5  $\mu\text{m}$ , respectively. The  $I_D$ - $V_G$  characteristics were measured with gate bias sweeps between -7 and 7 V. The source-drain voltage ( $V_D$ ) was fixed at 50 mV. The  $I_D$ - $V_G$  curve with a large hysteresis was observed. This hysteresis was caused by the injection of electrons and

holes into the Co-BND array. The shift of the  $I_D$ - $V_G$  curve in the positive voltage direction was caused by the injection of electrons into the Co-BND array, and the shift in the negative voltage direction was caused by the injection of holes into the Co-BND array. It was clearly observed that the hysteresis size of the  $I_D$ - $V_G$  curve increased with the number of Co-BND arrays, as designed.

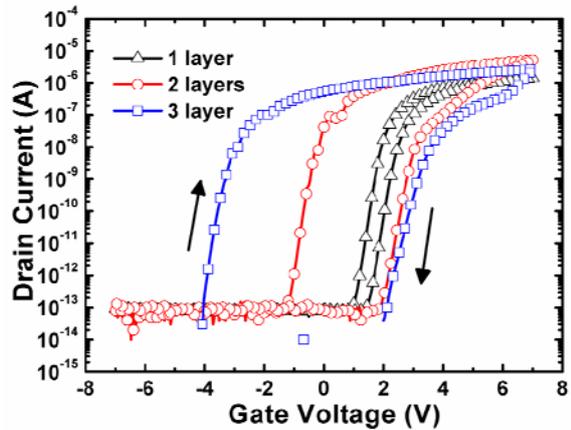


Fig. 1.3.  $I_D$  -  $V_G$  characteristics.

Figure 1.4 shows the writing and erasing characteristics of the memory with a multilayered Co-BND array. We measured the writing and erasing speeds by monitoring the threshold voltage shifts with different pulse widths at +5 and -5 V, respectively. An apparent threshold voltage shift was observed, and the threshold voltage shift saturated when the programming pulse was 100  $\mu\text{s}$  at +5 V. In addition, the threshold voltage shift was increased by stacking Co-BND arrays. The threshold voltage shift saturated when the programming pulse was 100  $\mu\text{s}$  at -5 V, the same as the writing characteristics. These results indicate that writing and erasing should be carried out for up to 100  $\mu\text{s}$  at  $\pm 5$

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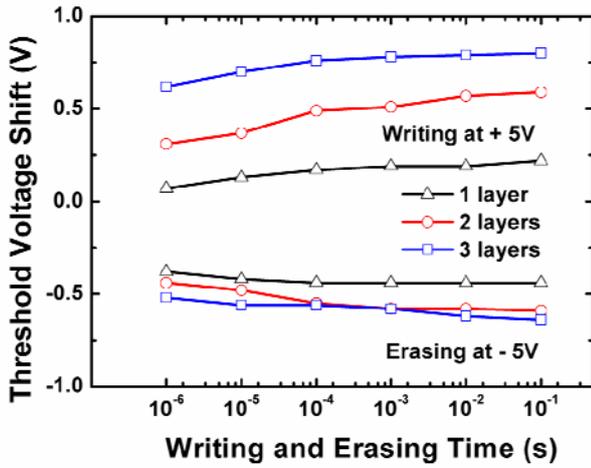


Fig. 1.4. Writing and erasing characteristics.

Figure 1.5 shows the charge retention characteristic of the memory with a multilayered Co-BND array. The charge retention characteristic was measured by monitoring the change in the memory window at +1.5 V after writing at +5 V and erasing at -5 V with a 100 ms pulsed bias. In the case of the memory with a single Co-BND array, the memory window disappeared for 100 s and the memory did not maintain the charges for  $3.1 \times 10^8$  s (10 years). However, the memory window remained after  $10^4$  s, and it is predicted that the memory window will remain unchanged after 10 years in the case of memories with multilayered Co-BND arrays. The window of the memory with a double-layered Co-BND array decreased from 5.1 to 3.1 V, which corresponds to 60% of the initial memory window. In the case of the memory with a triple-layered Co-BND array, the memory window decreased from 7.9 to 6.0 V, which corresponds to 76% of the initial

memory window. These results show that the retention characteristic of the memory was improved by stacking Co-BND arrays.

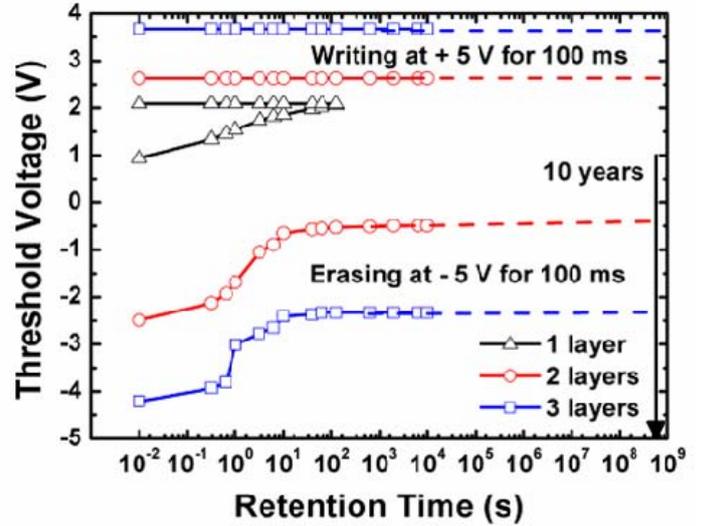


Fig. 1.5. Retention characteristic.

The window, better writing and erasing operations at low voltages, and the improvement of the retention characteristic of the memory with a multilayered Co-BND array can be explained on the basis of the band structure of the MOS structure. Figure 1.6 shows the band diagram of the memory. The band offset of  $\text{SiO}_2$  is 3.1 eV. However, the thickness of the tunnel oxide layer is 3 nm, and that of the  $\text{SiO}_2$  interlayer formed by Bio-LBL is 1.5 nm. The injection mechanism of electrons and holes is direct tunneling (DT). First, electrons and holes are injected into the first Co-BND layer from the Si conduction band by DT. Next, the applied electric field induces the injection of the electrons and holes in the first Co-BND array into the second Co-BND array by DT. The electrons and holes injected into the second Co-BND array are also injected into the third Co-BND array by DT. Therefore,

the electrons and holes are injected into the first, second, and third Co-BND arrays, and the numbers of electrons and holes are increased by stacking Co-BND arrays. The numbers of electrons and holes injected into a Co-BND array also increase at the same pulse voltage and width because the adsorption density of the Co-BND array acting as a charge storage site increases.

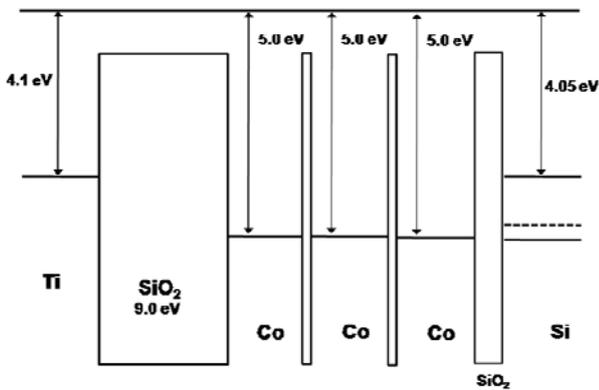


Fig. 1.6. Band structure of memory.

The work function of Co (5.0 eV) is positioned at the valence band of Si energy bands. The back-tunneling of electrons from the Co-BND array to the Si substrate is very difficult because the depth of the potential well between the work function of the Co-BND array and the Si conduction band is very large. Therefore, the retention of electrons is very good even in the memory with a single-layered Co-BND array. On the other hand, the holes injected into the Co-BND array back-tunnel to the Si substrate easily because the work function of the Co-BND array is positioned at the same level as the valence band of the Si substrate. However, holes are injected into the second or third Co-BND array in the case of the memory with a multilayered Co-BND array.

The holes injected into the second and third Co-BND arrays remain in the first and second Co-BND arrays when the holes try to back-tunnel to the Si substrate. Therefore, the holes do not back-tunnel to the Si substrate very easily and the retention characteristic of the holes is improved by stacking Co-BND arrays.

We proposed a nanodot-type floating gate memory with a multilayered nanodot array formed by Bio-LBL using TBF. High-density Co-BND nanodot arrays were stacked by Bio-LBL. In addition, each Co-BND was separated by the SiO<sub>2</sub> layer formed by PECVD and TBF biomineralization. The memory with a triple-layered Co-BND array embedded in the SiO<sub>2</sub> layer exhibited distinct  $I_D-V_G$  characteristics with a large hysteresis. The width of the hysteresis of the memory was increased by stacking Co-BNDs arrays. The writing at +5 V and erasing at -5 V were carried out for up to 100  $\mu$ s. The large memory window was predicted to be retained even 10 years after writing and erasing. These results demonstrate that the characteristics of the nanodot-type floating gate memory can be improved by stacking metal-nanodot arrays by Bio-LBL. In addition, the fabricated memory is promising for use as the future nanodot-type floating gate memory with a high performance and a good charge retention characteristic.

## 2. Guided Filament Formation in NiO-ReRAM by Embedding Gold

## Nanoparticle

Resistive Random Access Memory (ReRAM) has been attracting great attention as promising next generation memory which realizes memory cell size scaling down and low power operation. However, the mechanism of Re-RAM is not yet fully understood. The difficulty of finding mechanisms is partially attributed to a size of nanoscale switching region. In the case of a NiO based ReRAM, it is proposed that a resistive change occurs by a formation and rupture of conductive nanoscale filaments in NiO film. An initial electroforming step is required to activate the switching property and a nonpolar-type ReRAM required a high forming voltage. It was reported that soft breakdown occurred at the forming process by an electric field, which forms crystalline defects and/or grain boundaries in a metal oxide film and make a percolative path of the filaments. According to the proposed resistive switching mechanisms, it is supposed that many conductive filaments are randomly formed by the voltage stress inside the NiO matrix.

Filament type resistive switching has several merits, such as a large off/on resistance ratio and good retention. Despite these good memory properties, NiO based ReRAM has two critical problems to be solved. First place is the reduction of a high forming voltage. The memory cell should be on state to a low-resistance state by a low forming voltage. Second is the control the position of the nanoscale filament formation, which is a key to increase the memory capacity by defining

the memory bit positions. The nanoscale filament makes it difficult to control the precise positioning. To address these issues, the control of the electric field generated by the applying voltage is essential. Previously, resistive memories with metal nanoparticles embedded in oxide film have been reported. The conductive metal nanoparticles enhance the electric field in their vicinity, which was anticipated to define the conductive filament precisely. In these reports, however, metal nanoparticles were used only as nanoelectrodes. It was also true that nanoparticle placement with nanometric precision is hard to be carried out.

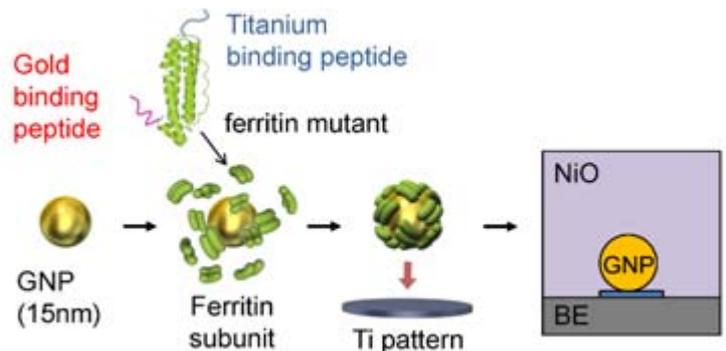


Fig. 2.1 Schematic image of bifunctional protein-based encapsulation/delivery system for nanoscale positioning of a GNP on bottom electrode (BE).

We have been studying biological nanofabrication method, which was named “Bio-nano-process (BNP)”. The BNP demonstrated that a single nanoparticle was selectively deposited at the designed positions and hexagonally closed packed nanoparticle array was formed based on the self organization of proteins. Various applications using BNP have been reported such as nano-dot floating gate memory, single electron transistor, position control of

carbon nanotube and crystallization of amorphous Si film.

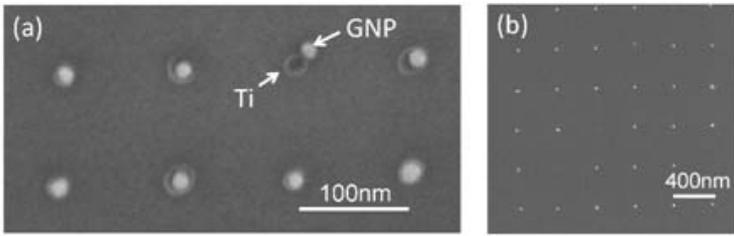


Fig. 2.2 SEM images of controlled placement of the GNP on bottom electrode before NiO deposition. (a) The selectively placed GNPs on Ti nanodisk with 100 nm pitch and (b) 400 nm pitch on  $n^+$ Si substrate.

In this study, we apply the BNP to incorporate GNP in the NiO matrix at the designated position and investigated the effect of electric field confinement by the GNP on the ReRAM properties. The effect of the GNP on the NiO matrix crystallinity was also investigated, which revealed that the GNP plays more than simple nanoelectrodes. Strong electric field should be generated at confined nanometric region in the vicinity of GNP in NiO matrix. However, the GNP in our study is not only used to concentrate an electric field by the nanoelectrode but also used to form defects in NiO layer and assist the forming process.

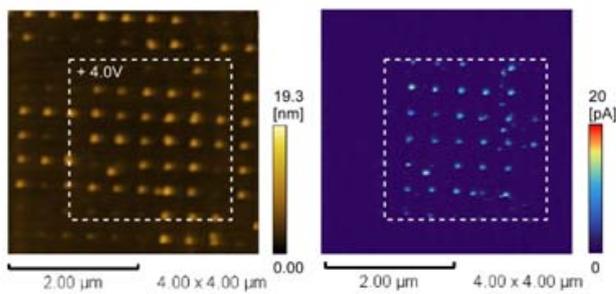


Fig. 2.3 Topographic image of c-AFM (Left) and corresponding current image (Right) scanned at  $V_{read}$  (-1.5 V) after scanned inside the dashed square area with applying at  $V_{set}$  (+4.0 V). The GNP

At first, we implement c-AFM to study the local conductivity of the GNP embedded NiO film. We initially aligned GNPs (diameter of 15 nm) with 400 nm pitch on bottom electrode ( $n^+$ Si) using a porter-protein. The porter-protein is a recombinant bifunctional protein made of a ferritin subunit, having gold-binding peptide and Ti-binding peptide at the C- and N-termini, respectively. The GNP is encapsulated by porter-protein and delivered to designate position (Fig. 2.1). Figure 2.2 shows SEM image of aligned GNPs before NiO deposition. The detailed process is described by Zheng *et al.* Then, the NiO film with 20 nm was evaporated on the GNP/ $n^+$ Si substrate. The c-AFM measurements were conducted using a PtIr coated tip, which is grounded. In this measurement, the SET ( $V_{set}$ ), RESET ( $V_{reset}$ ) and reading voltage ( $V_{read}$ ) were set at +4.0V, -2.5 V and -1.5 V, respectively. Figure 2.3 shows a topography and electrical data of the c-AFM experiment, where first a  $2 \times 2$  μm square area (inside the dashed line) was scanned with a sample bias of  $V_{set}$  and then whole area ( $4 \times 4$  μm large area) was scanned with  $V_{read}$ . The current image inside the dashed square area showed the conductive spots corresponding to the topographic image in Fig. 2.3. Whereas, no highly conductive spots were observed outside the  $2 \times 2$  μm square area. From the current mapping, the diameter of the conducting spot was about 60–100 nm.

Therefore, we assume that the spot contains multiple filaments. This result also indicates that the NiO film above the GNP is more easily formed conductive filaments with the lower voltage than other areas.

Figure 2.4 (a) shows current images scanned with  $V_{\text{read}}$  after set process. Three conductive spots were observed with 400 nm pitch. After reading the ON state sample, the center square area ( $200 \times 200$  nm) was scanned at  $V_{\text{reset}}$ , and then it was read again with  $V_{\text{read}}$ . The result is shown in Fig. 2.4 (b). The c-AFM image clearly shows that the conductive spot at the center of image disappeared. The result indicated that the filament was ruptured and turned OFF state. Finally, whole area was scanned at  $V_{\text{set}}$  and read again. The conductive spot in the center of image was formed again. As a result, a bipolar switching was confirmed. The switching area was confined only above the GNP which is different from the previous reports in c-AFM measurement of transition metal oxide materials where an entire written area (SET area) is conductive. Therefore, by using selectively positioned GNPs, the writing and erasing were achieved on defined area on the nanometer scale. These nanoscale switching is also promising for device scaling.

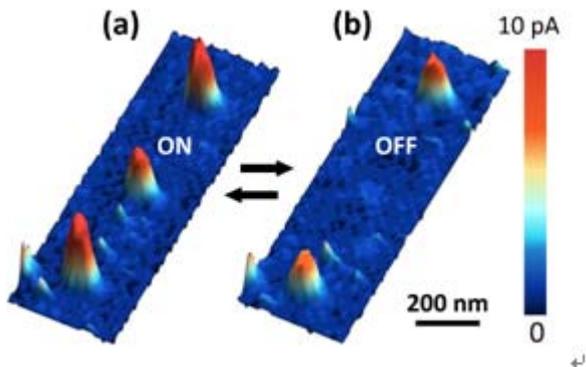


Fig. 2.4 C-AFM images of NiO surface scanned at  $V_{\text{read}}$  (-1.5 V) after set scan. The GNP was aligned with 400 nm pitch. (a) Three conductive spots shows ON state. (b) Current image reading with  $V_{\text{read}}$  after switched off only the center spot by scanning at the center area with applying RESET voltage (-2.5 V).

In order to study the effects of the GNP further in memory switching, Pt/NiO-GNP/Pt structure and Pt/NiO/Pt structure were produced. The GNPs coated by porter-protein were randomly adsorbed onto the Pt bottom electrode. The proteins were removed using UV/Ozone treatment. Then, NiO film (30 nm) was deposited on the GNP/Pt bottom electrode. Finally, Pt top electrodes with a diameter of 100  $\mu\text{m}$  were formed. Figure 2.5 (a) and (b) shows the typical current-voltage relationship ( $I$ - $V$ ) of sample with and without the GNP, respectively. After the first voltage sweep (electroforming process), both samples exhibited nonpolar resistive switching behaviors. The average forming voltage was +5.8 V and the set voltage was +1.9 V for the sample without GNPs, while the forming and the set voltages were +2.5 V and +1.8 V for the NiO with GNP. As shows in Fig. 2.5 (a) and (b), the forming voltage is reduced to the nearly same level of the set voltage. In many resistive switching materials, a forming process is needed to transit an initial device into a switching state. However, the sample with the GNP shows relatively lower forming voltage. On the other hand, no distinctive effects were observed in SET and RESET switching after the first voltage sweep. This indicates that

the GNP has no influence on the set and reset operation in our structure.

To elucidate the conduction mechanisms of the Pt/NiO-GNP/Pt memory cell, the  $I$ - $V$  curves were replotted in a  $\text{Log-Log}$  scale (Fig. 2.5 (c)). Additionally, the differential resistances  $d\text{Log}I/d\text{Log}V$  derived from  $\text{Log}I$ - $\text{Log}V$  measurement at the forming process were plotted in Fig. 2.5 (d). As shown in Fig. 2.5 (c), the conduction behaviors at the low voltage region is similar even GNPs were existed because the slope of approximately 1.0 at the low voltage region. This conduction behavior can be explained by ohmic conduction. However, at the high voltage region ( $> +2.0$  V), the conduction mechanism is completely different between the sample with and without GNPs (Fig. 2.5 (d)), because the slope of the  $\text{Log}I$ - $\text{Log}V$  curvature in the GNPs embedded sample increase differently. In the case of the memory cell without the GNP, the nonlinear relation of the  $\text{Log}I$ - $\text{Log}V$  plot at high voltage region is attributed to the Poole-Frenkel conduction. According to the P-F conduction, a plot of  $\text{Log}I/V$  vs  $V^{1/2}$  has linear relation. This P-F model is good agreement with the result of  $I$ - $V$  curve of the sample without the GNP. On the other hand, in the sample with the GNP, the slope drastically increases at a higher voltage starting from around  $+2.0$  V (Fig. 2.5 (d)). This conduction behavior might be attributed to the concentration of an electric field on the GNP and/or effects of defects or grain boundaries in NiO film placed above the GNP.

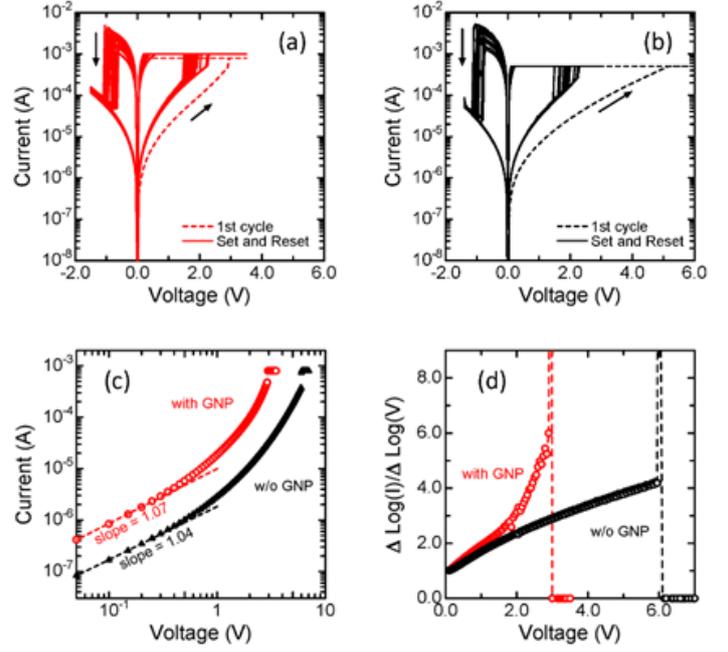


Fig. 2.5 Typical  $I$ - $V$  characteristics of (a) the GNP embedded ReRAM and (b) without GNP. (c) The  $\text{Log}I$ - $\text{Log}V$  plot at the forming process of NiO resistive memory with and without GNP. (d) The differential resistance  $d\text{Log}I/d\text{Log}V$  plot against voltage at the forming process. The curvature of the  $\text{Log-Log}$  plot increases differently at the high voltage region.

The relationship between a forming voltage and an initial resistance of the memory cell is shown in Fig. 2.6. The initial resistance is reduced by one order of magnitude due to the effects of the GNPs compared to the initial resistance of the sample without GNP. The resistance of NiO film is related to an oxygen composition in NiO.<sup>30</sup> and a crystal quality of the film. Even the deposit condition of NiO film is same each other, the crystallinity of the NiO film may be different in these two films. To understand the mechanism of the reduction of the forming voltage, the crystalline structure was observed using a

cross-sectional TEM image. Figure 2.7 shows the cross-sectional TEM image before a top electrode formation. The NiO region without GNP has a fine columnar structure (5-10 nm) with a flat surface. On the other hand, as is evident from the TEM image, the convex structure was observed on the top of the NiO where the GNP is located. The NiO on the GNP contains smaller size of grains. The irregular grain structure on the GNP gives rise to the increase of grain boundaries and defects in NiO film. We estimate that these grain boundaries and defects in NiO were introduced during the deposition of the NiO layer on the GNP.

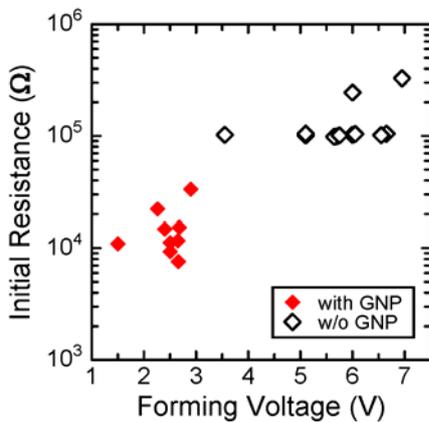


Fig. 2.6 Relation between the forming voltage and the initial resistance with and without GNPs. The forming voltage was reduced and the initial resistance also was decreased by the GNP.

It was reported that the nanoscale filament paths that are made of a nickel are formed at the grain boundary. Since grain boundaries are more conductive than other regions and the grain boundary acts as a leakage source, the lower initial resistance of the memory cell with the GNP is contributed to the leakage current of the

grain boundaries and defects above the GNP. Additionally, it is expected that the lower forming voltage can be mainly attributed to the creation of filament paths caused by the defects in NiO film rather than concentration of electric field at locally placed onto the GNP. Therefore, the most significant factor in the decrease of the forming voltage was due to the defects in the NiO layer formed by the GNP. That is, the highly conductive defects in NiO might assist the formation of conducting filaments at the forming process. The GNP might act as a defect creator during the fabrication process. In other words, a conventional forming process can be explained that a voltage stress make a grain thinner or smaller than those of an as-grown film. Although some defects assist the formation of conducting filaments at the forming process, the SET and RESET voltages were similar to each other even the GNP is embedded. This means that the switching region might be confined in nanoscale regions and smaller than the size of the GNP.

According to these results, the role of the GNP was understood as causing the following phenomena. In the electroforming process, the conducting filaments were easily formed with a lower voltage owing to the preexisting defects above the GNP and electric field enhancement by the GNP. At the reset process, conducting filaments ruptured at the interface between Pt top electrode and NiO. However, the filaments are partially remained in the NiO above the GNP. After that, partially remained conductive filaments connect again at the set process.

nano-scaled structure for new memory device applications.

#### Acknowledgements

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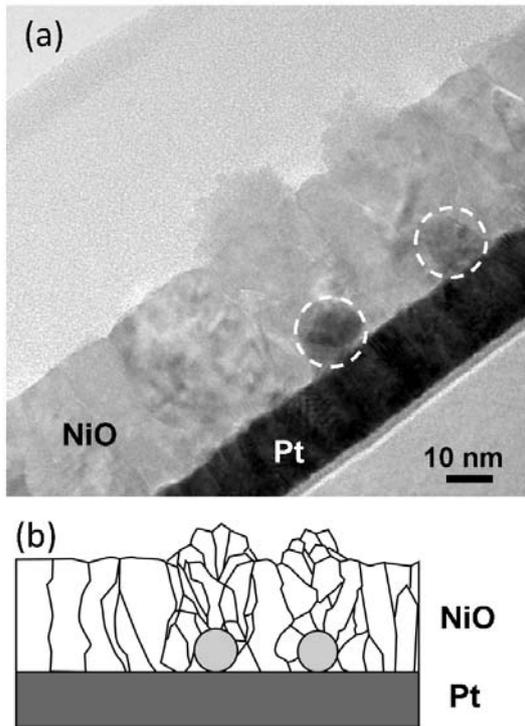


Fig. 2.7 (a) Cross-sectional TEM image of the GNP embedded NiO-GNP/Pt structure before top electrode formation. The thickness of NiO film was 30 nm. (b) Schematic image of cross-section of the device with the

We demonstrated the GNP embedded NiO-based ReRAM devices using BNP. The location of conducting filament formation was controlled to be at the position of the GNP and the writing and erasing were achieved on defined area on the nanometer scale. The forming voltage was decreased according to the defects at highly localized region. The cross-sectional TEM image strongly supported that the grain structure is contributed to decrease the forming voltage. This technique can be used for the direct observation of filament path. Additionally, we can design various nano-elements using BNP. Therefore, BNP could represent a significant advancement toward developing