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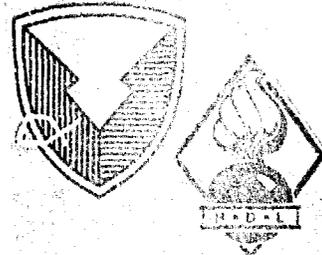


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# A Preliminary Examination of "Y1" (a Proprietary Thin-Film Ferroelectric Produced by Symetrix Corporation)

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13. ABSTRACT (Maximum 200 words) <p>This report presents the results of several tests of the ferroelectric thin film, designated "Y1," which was developed by Symetrix Corporation. The tests include fatigue, at room temperature and 125°C, to greater than <math>2 \times 10^{11}</math> cycles; retention for short periods of time (up to 1000 s) at room temperature and 125°C; retention after fatigue; voltage dependence of retained polarization from 1.5 to 8 V; and write pulse-width dependence of retained polarization from 50 ns to 500 ms. While these tests address critical issues for nonvolatile memory applications, they were limited by a time constraint of one week, and more testing is needed.</p>				
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# 1. Introduction

This report presents the results of a preliminary investigation of one of the promising ferroelectric (FE) thin films reported at the International Symposium on Integrated Ferroelectrics (ISIF), Monterey, CA, in March 1992. This electrical evaluation of the FE material was performed at the request of, and with the support of, the Defense Advanced Research Projects Agency (DARPA). The radiation tests on the "Y1" material were performed for the Defense Nuclear Agency (DNA).

Because of the highly proprietary nature of Y1, the electrical evaluation performed at the Harry Diamond Laboratories (HDL) was limited to one week, 18-22 May 1992. During the entire test period a representative of Symetrix Corp. was present at HDL to observe the testing procedures and control the Y1 material.

The findings in this report are in no way conclusive about the performance of the Y1 material as a storage cell for nonvolatile memory applications (the primary proposed application of the material), or about the long-term stability, manufacturability, or many other important parameters relating to FE thin films. Other shortcomings of this preliminary report are as follows:

- (1) No information about the repeatability of the experiments was obtained; each test was performed only once, and only five FE capacitors were tested.
- (2) The compatibility of Y1 with state-of-the-art integrated circuit (IC) technologies and fabrication techniques (thermal anneals, passivation, metalization, etc) is unknown and could not be determined.

# 2. Ferroelectric Y1 Test Samples

For the Y1 evaluation, Symetrix provided the following: three wafers partially processed through FE capacitor top electrode; one quarter of a fully processed wafer (through third-level metal) with bond pads; and halves of two partially processed wafers. The fully processed quarter wafer and the two partially processed wafer halves were diced and packaged at HDL. Because we were not permitted to dice or package any of the three partially processed wafers, only limited probe measurements are presented.

The two wafer halves contained simple capacitor structures consisting of Pt top and bottom electrodes with a Y1 thin film between them. To package and bond these devices, it was necessary to etch the Y1 from a small corner of each die to contact the bottom electrode. The gold bond wires were then attached directly to the top electrode of the capacitor structures and to the exposed bottom electrode. Only  $100 \times 100 \mu\text{m}$  capacitors were packaged from these samples (because of the necessity of bonding directly to the top electrode).

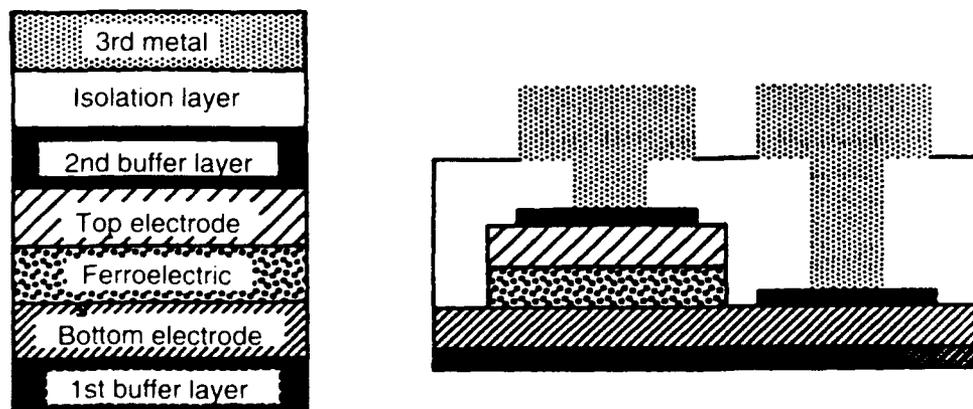
The quarter wafer had an array of capacitors with various areas processed through third-level metal, with bond pads for both the top and bottom electrodes. Figure 1 shows both the capacitor stack and the bond pad connections. From this wafer slice  $20 \times 20 \mu\text{m}$ ,  $30 \times 30 \mu\text{m}$ , and  $100 \times 100 \mu\text{m}$  capacitors were packaged. The bulk of the evaluation was performed on these packaged samples.

### 3. FE Capacitor Packaging

The details of the packaging on the Y1 samples are as follows:

- (1) Each wafer was mounted in a frame for the Micro-Automation wafer saw using Mylar mounting tape.
- (2) The framed wafer was mounted on the saw chuck and diced into packageable chips.
- (3) Individual die were removed from the Mylar tape.
- (4) The Y1 was etched down in one corner of each chip using straight HF to expose the bottom electrode on the die from the partially processed wafer halves (no bonding pads).

Figure 1. Y1 cross section processed through third metal and resulting patterned capacitors (figure provided courtesy of Symetrix Corporation).



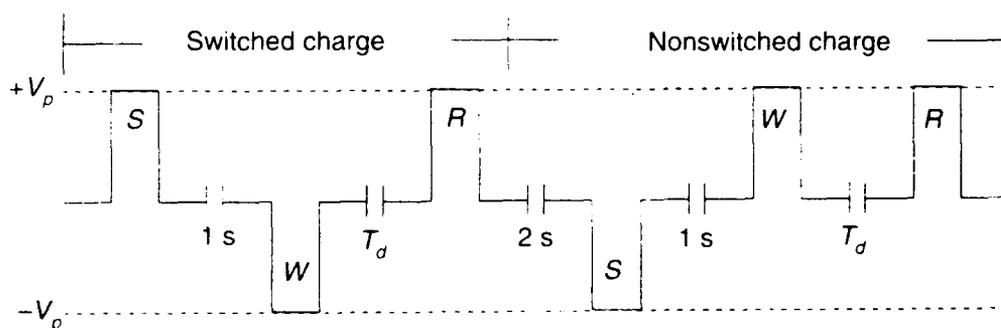
- (5) The individual chips were mounted in 16 pin dual in-line packages (DIP's) using DITAC (a thermoplastic adhesive) at 150°C.
- (6) Each chip was wire lead bonded on a thermosonic bonder at 150°C using 1-mil gold wire. One bond was made to the bottom electrode on each chip, through a bond pad on the fully processed samples and directly to the bottom electrode on those that were etched down.

## 4. Electrical Tests

The primary test used in this evaluation was a measurement of the retained polarization (this is the amount of charge that would be available to discern the stored memory state in a nonvolatile memory cell), denoted as  $\Delta P$ , measured 1 s after a poling (write) pulse (see pulse train in fig. 2). This measurement was performed in two steps by first measuring the switched charge and then measuring the unswitched charge. The switched charge was measured as follows: (1) poling an FE capacitor with a positive voltage pulse (as a set pulse), and after 1 s a negative voltage pulse (the write pulse); (2) waiting 1 s, or for retention measurements, the appropriate retention time; and (3) reading the stored polarization by poling the capacitor with a positive voltage pulse and recording the voltage that appeared across the integrating capacitor. Similarly the unswitched charge was measured by (1) poling the capacitor with a negative voltage pulse (a set pulse) and after 1 s applying a positive pulse (the write pulse), (2) waiting 1 s, and (3) reading the stored polarization by poling with another positive voltage pulse and again recording the voltage that appears across the integrating capacitor. The retained polarization is found by subtracting the polarization measured in the unswitched case from the polarization measured in the switched case.

Notice that the polarity of the set pulses applied before each write pulse was of the opposite polarity of the following write pulse. This

Figure 2. Standard pulse train used to measure retained polarization.

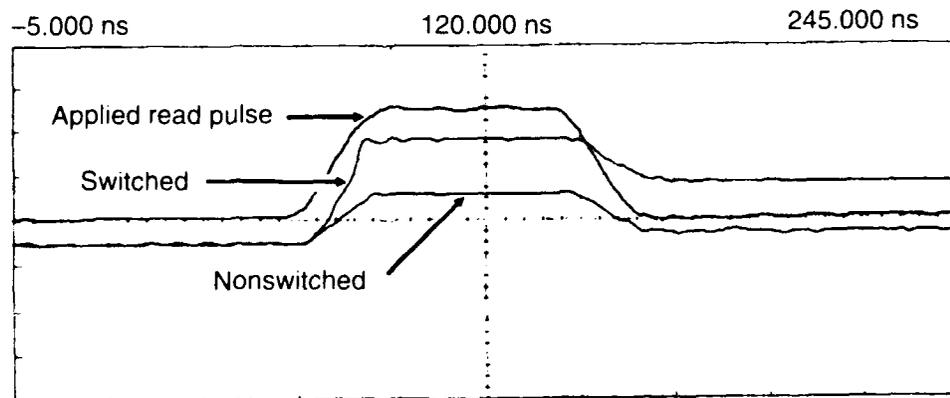


procedure was used to provide a "worst case" condition for each write. The set pulses ensure that both positive and negative write pulses have to switch the FE polarization and not "pump up" an existing polarization state. For good quality capacitors (high retained polarization and little fast polarization decay), the presence or absence of set pulses was found to have a very small effect on measurement results. However since we were dealing with a new (and unknown) material, we tried to be as cautious as possible in our a priori assumptions.

This measurement gives an estimate of the amount of signal (expressed in  $\mu\text{C}/\text{cm}^2$ ) that could be used in a memory application to sense the difference between a stored 1 and 0. At least  $1 \mu\text{C}/\text{cm}^2$  of retained polarization has been required for nonvolatile memories designed with PZT as the FE film. Figure 3 shows an example of the signal traces obtained during a representative retained polarization measurement. Shown in the figure are a positive voltage pulse applied as a read pulse and the voltages appearing on the integrating capacitor during the read for the switched and unswitched cases.

Most of the measurements on the packaged parts were performed on the  $30 \times 30 \mu\text{m}$  capacitors. The standard test conditions for these parts were 50-ns-long write/read pulses with 20-ns risetimes. The  $\pm 5.0\text{-V}$  pulse amplitudes across the FE capacitor were achieved by applying  $\pm 5.2\text{-V}$  pulses across the FE capacitor/integrating capacitor series circuit to compensate for the small voltage drop across the integrating capacitor. The sense capacitor used for these samples was 470 pF.

Figure 3. Example of raw data obtained for retained polarization measurement.



<b>Function 2</b>	<b>= 2.000 V/div</b>	<b>Offset</b>	<b>= 0.000 V</b>
Timebase	= 25.0 ns/div	Delay	= 120.000 ns
Memory 1	= 150.0 mV/div	Offset	= 100.0 mV
Timebase	= 25.0 ns/div	Delay	= 120.000 ns
Memory 2	= 150.0 mV/div	Offset	= 100.0 mV
Timebase	= 25.0 ns/div	Delay	= 120.000 ns

One test was performed using packaged  $100 \times 100 \mu\text{m}$  capacitors from one of the partially processed wafers. For this test, the pulse widths were 100 ns and had 20-ns risetimes. Again, the pulses had 5.0-V amplitudes across the FE capacitor. The sense capacitor used was 3.3 nF.

Wafer level tests were also performed on  $100 \times 100 \mu\text{m}$  capacitors from one of the three partially processed wafers. The retained charge measurements were performed using 2- $\mu\text{s}$  write/read pulses with 500-ns risetimes with a 3.3-nF integrating capacitor. The long write/read pulses and slow risetime were required because of the long lead length and parasitic capacitance of the probes. We felt it was important to perform these tests to ensure that the packaging steps did not significantly affect the performance of the Y1 samples. Unfortunately we were not able to probe smaller samples because of the limitations of our present probe setup; however, a new probe station will be available shortly.

## 5. Test Results

Because of the time limitation of the electrical evaluation, we were only able to perform a limited number of tests, and in many cases only one or two samples were used in each test. We (as well as our sponsor) felt that the most important tests were fatigue and retention; unfortunately, these are also the most time consuming to perform. The following sections describe the results from each test.

### 5.1 Room-Temperature Fatigue

A  $30 \times 30 \mu\text{m}$  capacitor from the fully processed wafer was used to measure the effects of repeated cycling on the retained polarization. The fatigue pulses, shown in figure 4, were the same 5-V, 50-ns-wide, 20-ns-risetime pulses that are used in measuring the retained polarization. The 50-ns pulses were followed by 30-ns delay times (at 0 V) for a total period of 250 ns and a fatigue cycling frequency of 4 MHz. The polarization measurements were made by intermittently (approximately with log time) stopping the cycling and using the standard test pattern (described above) to measure the retained polarization.

Figure 5 shows the retained polarization as a function of cycles to  $2.8 \times 10^{11}$  read/write cycles. Along with the 1-s retained polarization, the switching and nonswitching voltages measured across the sense capacitor are also shown. The only noticeable effect of this fatigue cycling was a slight increase in the retained polarization early in the fatigue test. Note that the voltages measured across the sense capaci-

Figure 4. Pulse waveform used to fatigue Y1 capacitors.

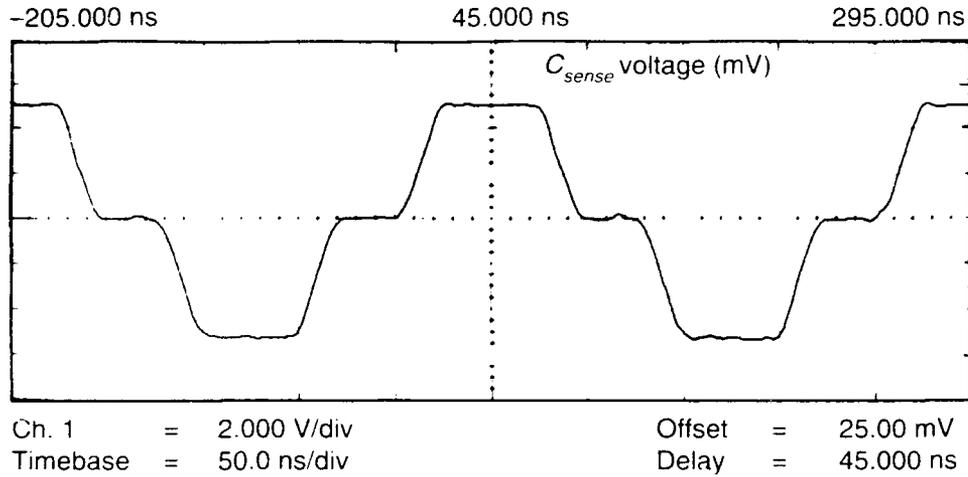
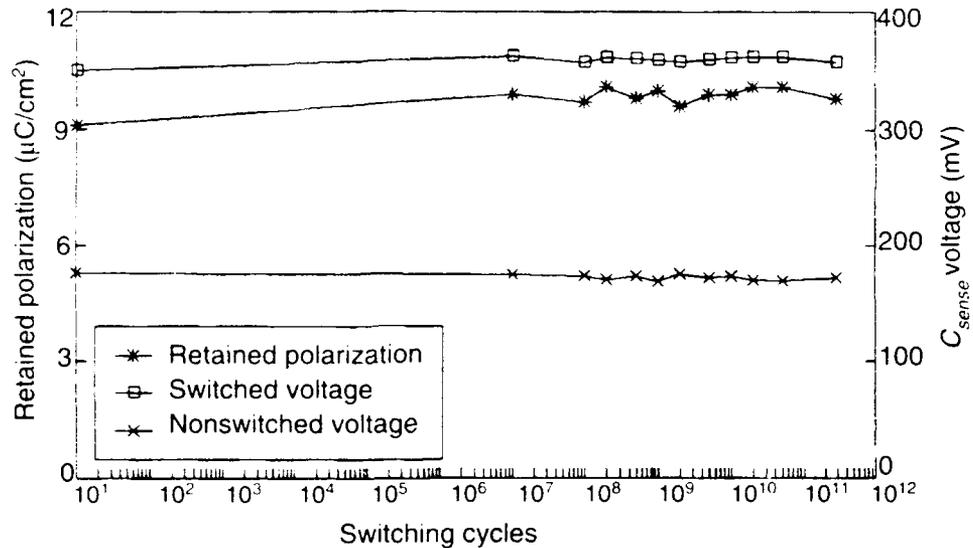


Figure 5. Retained polarization versus number of cycles (at room temperature and using waveform shown in fig. 4). Notice that there is actually a slight increase in retained polarization at over  $1 \times 10^{11}$  cycles.



tor did not change, most likely indicating that the dielectric constant was not affected by fatigue.

## 5.2 High-Temperature Fatigue

A new Y1 capacitor sample was used to measure fatigue at  $125^\circ\text{C}$  (the upper end of the military specification temperature range). The 1-s retained polarization of the sample was measured to be  $10.0 \mu\text{C}/\text{cm}^2$  at room temperature before heating. The sample was then mounted inside an oven using a fixture whose leads passed through a port in the oven to a sense capacitor mounted outside (the total lead length from sample to sense capacitor was approximately 2 in.,

and the sense capacitor was kept at approximately room temperature). The circuit was connected to a pulse generator through 1 ft of 50- $\Omega$  coaxial cable. This arrangement increased the circuit ringing slightly but, in our opinion, not enough to affect the fatigue test. After the oven temperature was stabilized at 125°C (approximately 5 min) the 1-s retained polarization was measured to be 5.3  $\mu\text{C}/\text{cm}^2$ .

The fatigue pulses for the high-temperature fatigue were the same as those used for the room temperature fatigue test (see above). The results in figure 6 again show no significant effects on the retained polarization from repeated cycling. The retained polarization after  $2.5 \times 10^{11}$  cycles is 5.5  $\mu\text{C}/\text{cm}^2$  measured at 125°C, slightly greater than the initial polarization; as before, there was no evidence of a decrease in the film dielectric constant.

### 5.3 Room-Temperature Retention

A fresh Y1 capacitor was selected to test the short-term retention capability of this material. Again, the standard measurement pulse train was used (as in the retained polarization measurement; see fig. 2) but the time delay between the write pulses and the read pulses was varied from 1 s up to 1000 s. For each measurement point, both the retained polarization and the switching and nonswitching sense capacitor voltages were measured from the integrating capacitor.

Figure 7 shows a small decrease in the retained polarization from 10.0  $\mu\text{C}/\text{cm}^2$  at 1 s (write/read delay) to 9.2  $\mu\text{C}/\text{cm}^2$  at 1000 s. Unfortunately 1000 s is much too short a time period to make any predic-

Figure 6. Retained polarization versus number of cycles, fatigued and measured at 125°C.

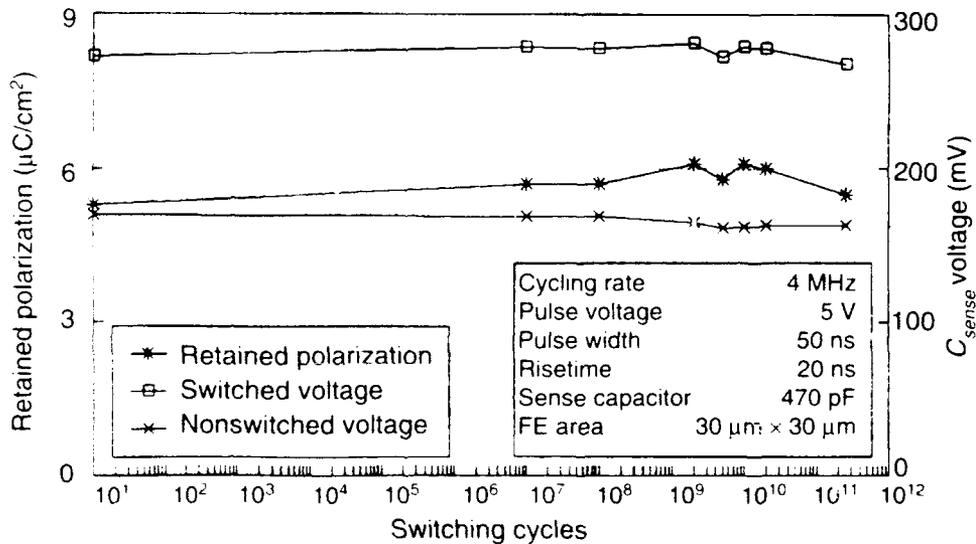
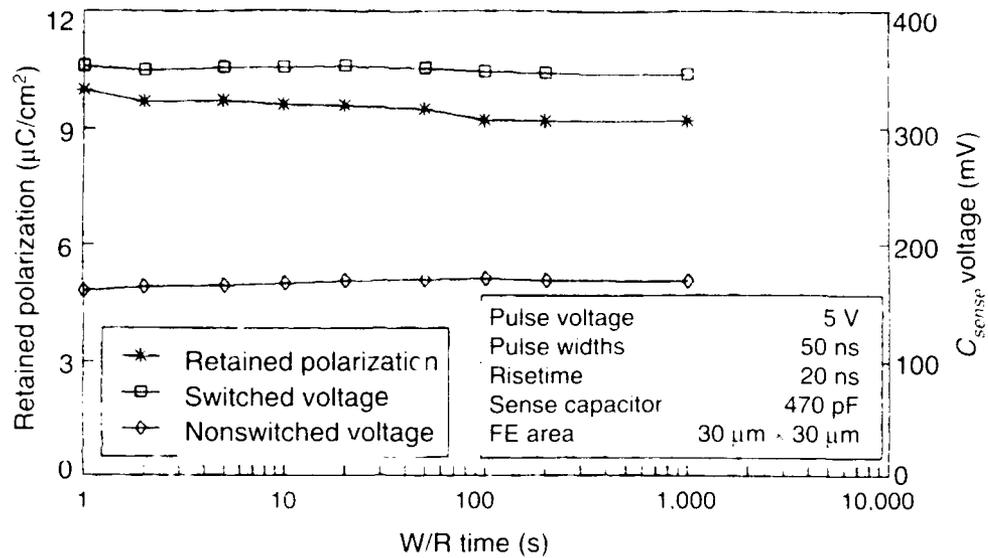


Figure 7. Retained polarization (room temperature) as a function of write/read pulse delay time from 1 to 1000 s. Longer retention times could not be measured because of time constraint of experiments (see text).



tions or quality statements about the film at 1 or 10 years, which are more typical time period specifications that might be required for a memory device. Another item to notice from this figure is that both the switching and nonswitching voltages are contributing approximately equally to the loss of polarization. From the 1- to 1000-s measurements, the switching voltage decreases by 7.3 mV and the nonswitching voltage increases by 7.6 mV.

#### 5.4 Retention after Fatigue

Next, we measured the retention of the Y1 capacitor that was first fatigued to  $2.8 \times 10^{11}$  cycles at room temperature. This test was performed the same as the room-temperature retention test described above. Figure 8 shows the results for both the retained polarization and the sense capacitor voltages. These data show a decrease in the retained polarization from  $9.9 \mu\text{C}/\text{cm}^2$  at 1 s (write/read delay) to  $8.6 \mu\text{C}/\text{cm}^2$  at 1000 s. The polarization decay rate increased very slightly after fatigue compared to the decay rate of the nonfatigued sample. Again, this time period is much too short to make any predictions about the long-term retention of the film. As with the nonfatigued sample, the switching and nonswitching voltages are contributing equally to the loss of retained polarization.

#### 5.5 High-Temperature Retention after High-Temperature Fatigue

After the high-temperature fatigue was measured, the same sample was then used for a retention test while the temperature was still  $125^\circ\text{C}$ . This test was performed using the same pulses as the room-

temperature retention tests reported above except that the sample was still in the high-temperature test fixture described in section 5.2.

Figure 9 shows the results of this retained polarization and the voltages measured across the sense capacitor for both the switched and the nonswitched cases. The retained polarization is seen to decay from  $4.6 \mu\text{C}/\text{cm}^2$  at a write/read delay of 1 s to  $3.6 \mu\text{C}/\text{cm}^2$  at a delay of 1000 s at  $125^\circ\text{C}$ . This decay rate is approximately the same as that for the retention measurements made at room temperature for both the fatigued and nonfatigued samples. As with both room-

Figure 8. Retained polarization (room temperature) versus write/read delay time from 1 to 1000 s after first fatiguing to over  $2 \times 10^{11}$  cycles.

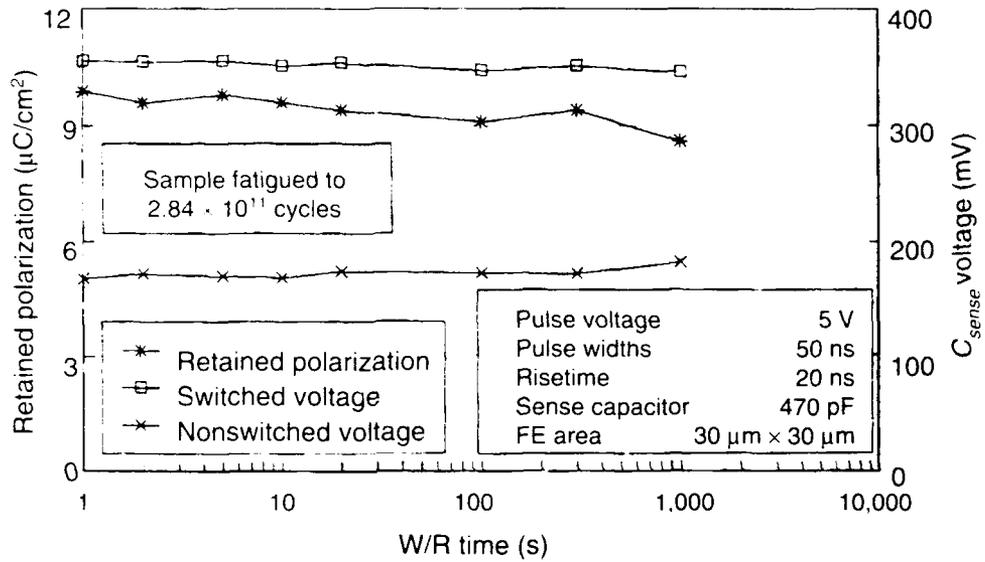
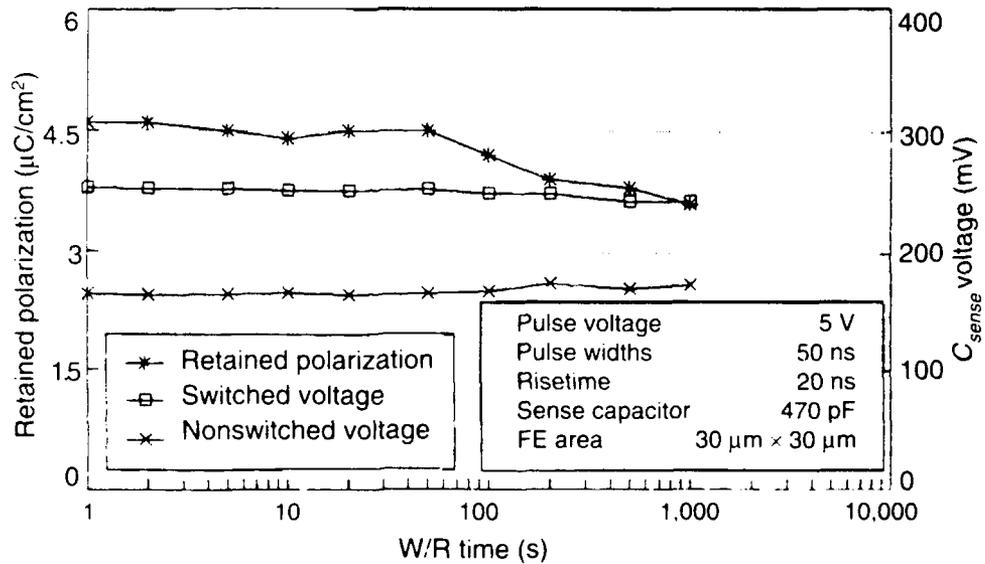


Figure 9. Retained polarization (measured at  $125^\circ\text{C}$ ) from 1- to 1000-s write/read delay times after  $2.5 \times 10^{11}$  fatigue cycles at  $125^\circ\text{C}$ .



temperature retention measurements, the switched and nonswitched measurements contribute equally to the decay of the polarization.

We repeated the above tests with the same sample after allowing the capacitor to remain at 125°C for 6 hr after the completion of the previous retention test (a total time at temperature of approximately 30 hr). The sample remained undisturbed for the 6 hr after having been last poled with a positive 5.0-V pulse. Figure 10 shows that the retained polarization at 1 s had dropped to 2.0  $\mu\text{C}/\text{cm}^2$  from its value of 4.6  $\mu\text{C}/\text{cm}^2$  in the previous test. The value was then constant for write/read delay times out to 1000 s but dropped to 1.4  $\mu\text{C}/\text{cm}^2$  for a delay time of 25,000 s. Although this test could possibly indicate a serious ageing problem for the Y1 material for long exposure at elevated temperatures, more measurements are required to determine the extent of the problem. Ageing here is being used to refer to losses of retained polarization over time while the ferroelectric is in a poled state.

## 5.6 Room-Temperature Retention after High-Temperature Fatigue

After the sample discussed above was cooled to room temperature, its retention was remeasured. The results in figure 11 show that the sample did not fully recover from the effects of being stressed at high temperature for a period of time (approximately 45 hr). Before the initial heating (and before fatigue), the sample had a 1-s retained

Figure 10. Retained polarization (measured at 125°C) from 1- to 1000-s write/read delay times after  $2.5 \times 10^{11}$  cycles and additional "ageing" for 6 hr at 125°C (total time at 125°C was 30 hr).

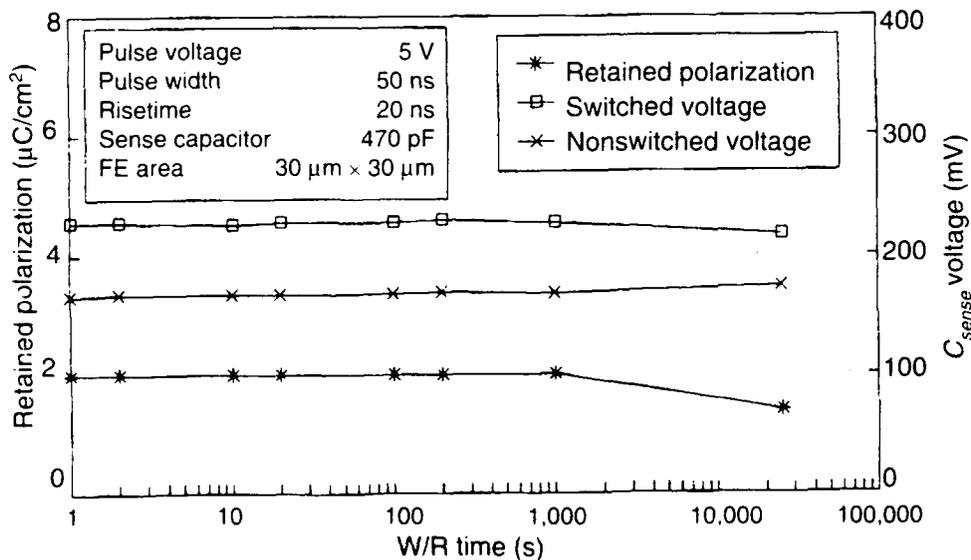
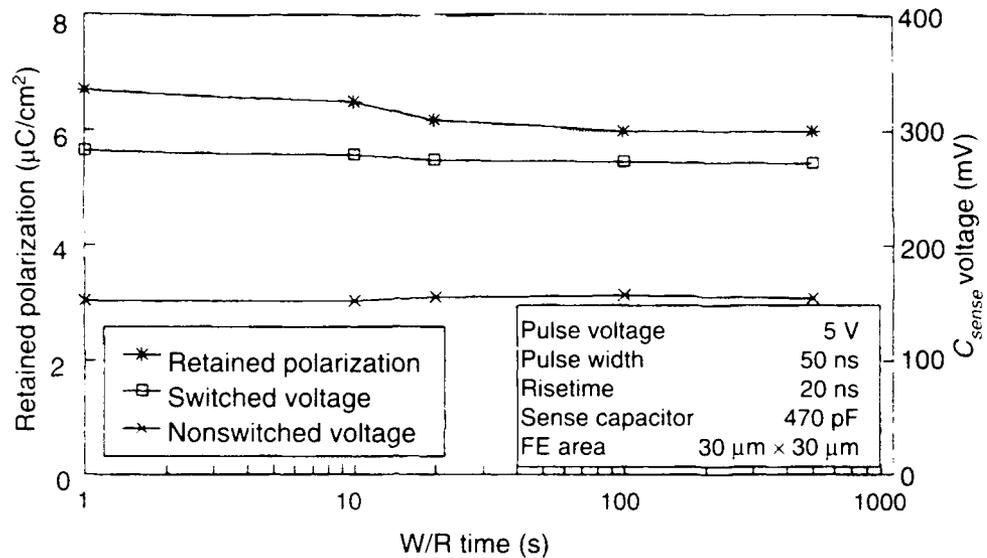


Figure 11. Retained polarization (room temperature) from 1 to 1000 s after stressing at 125°C.



polarization of 10.0  $\mu\text{C}/\text{cm}^2$ . After the temperature was stabilized at 125°C, but before cycling, the retained polarization was 5.3  $\mu\text{C}/\text{cm}^2$ , and after fatiguing to over  $2 \times 10^{11}$  cycles, the retained polarization increased slightly to 5.5  $\mu\text{C}/\text{cm}^2$ . After another 24 hr at 125°C, the 1-s retained polarization had dropped to 1.7  $\mu\text{C}/\text{cm}^2$ .

After the sample was returned to room temperature, the retained polarization at 1 s was only 6.7  $\mu\text{C}/\text{cm}^2$ , a drop of 3.3  $\mu\text{C}/\text{cm}^2$ . The sample then continued to lose polarization as the write/read time delay was increased, finally dropping to 6.0  $\mu\text{C}/\text{cm}^2$  at 500 s.

### 5.7 Write Pulse-Width Dependence

We also measured the effect of varying the write pulse width on the retained polarization at 1 s. The width of the set pulses and the width of the write pulses were varied together from 50 ns up to 500 ms. The results of the write pulse-width dependence measurement are shown in figure 12. The data show a slight increase in polarization with the increasing write pulse width that is essentially linear in log time.

This result indicates that there will probably not be a problem poling this material with short (<100 ns) write pulses that are necessary for high-speed memory operation.

### 5.8 Voltage Dependence

The effect of pulse amplitude on retained polarization was measured. The pulse voltages (write and read) were varied from 1.5 to

8 V. For this test, the given voltages are the voltages across both the FE capacitor and the sense capacitor. Figure 13 indicates that this material has a low and well-defined coercive field and that the material should perform well for pulse voltages down to 3.0 V.

## 5.9 X-Ray Radiation Response

A brief examination of the response of the Y1 material to 10-keV x-rays was also performed. Figure 14 shows the retained polarization versus total dose for a Y1 capacitor irradiated without applied bias but poled positive (with respect to the top electrode) during irradiation. The Y1 film showed a much larger degradation of the

Figure 12. Retained polarization versus write pulse width from 500 ns to 0.5 s (room temperature) using a constant 50-ns read pulse.

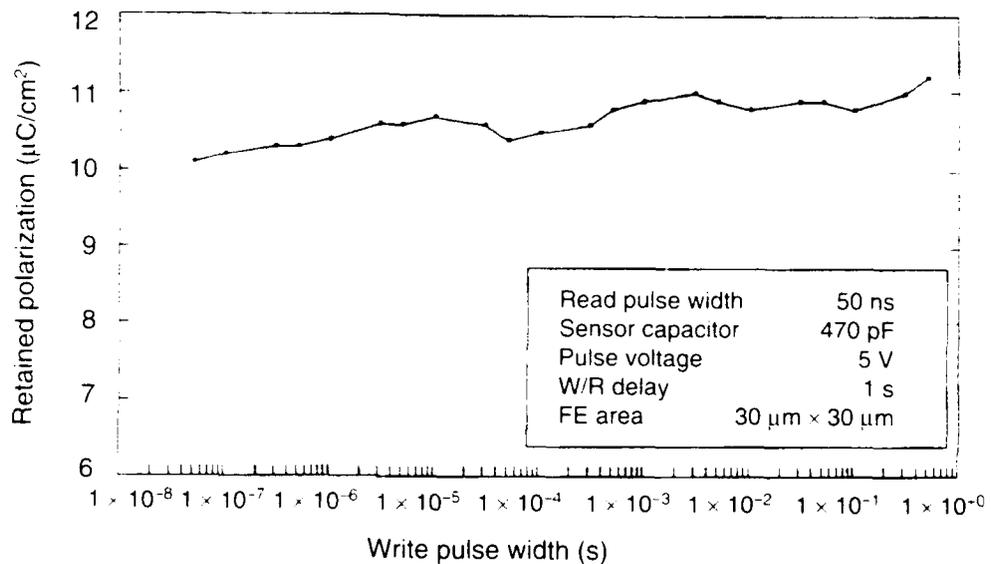


Figure 13. Retained polarization as a function of voltage. Both write and read voltages were varied in same fashion.

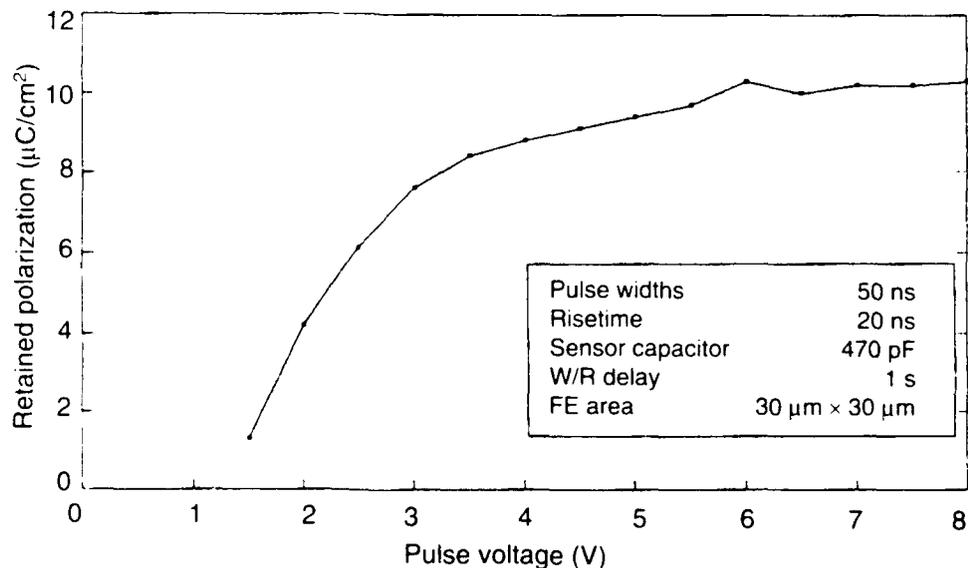
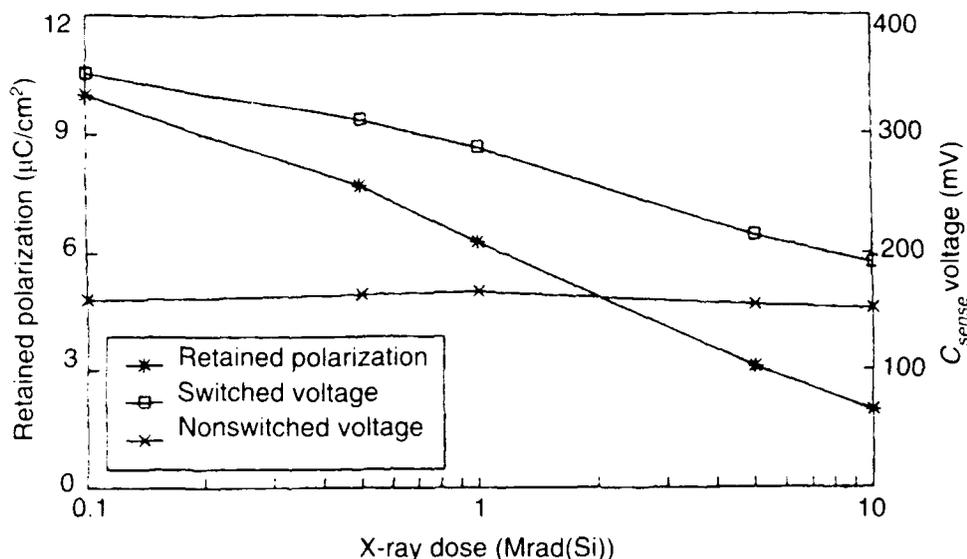


Figure 14. Retained polarization as a function of total dose ionizing (x-ray) radiation.



retained polarization than has previously been observed for PZT films. Although the polarization was sufficient for the device to operate as a nonvolatile memory element at 10 Mrad(Si) (a considerable total dose), these data indicate a need to examine the film under more rigorous conditions, including dose rate, applied bias, and temperature, as well as to examine more parameters than just retained polarization, e.g., fatigue, retention, imprint, etc.

## 6. Conclusions

In general, the proprietary Y1 FE film lived up to its "fatigue free" advanced billing. As pointed out, there are a number of serious shortcomings in this evaluation, mostly because of the time constraint imposed; these include the number of samples tested, the short time period of retention data, and the limited variety of electrical tests. Even so, the film shows considerable promise in that it appears that it can be switched with 50-ns pulses at room temperature and 125°C without significant fatigue of the retained polarization. One potential problem discovered during the short evaluation was a possible ageing phenomenon at elevated temperatures, although our data are incomplete at this time.

## Appendix A.—Test Summary

- 18 May 1992* Brad Melnick of Symetrix arrives with Y1 wafers. Two wafers taken to HDL SEMT for dicing, packaging, and bonding. Probe test of wafer W1\_1\_63 100 × 100 capacitor used to measure write pulse-width dependence. Probe test of wafer W1\_1\_63 measured fatigue.
- 19 May 1992* Packaged Y1 capacitors delivered by HDL SEMT. Sample 4\_30\_1 pin 3 used for write pulse-width dependence test. Sample 4\_30\_1 pin 2 used for voltage dependence test. Sample 4\_30\_1 pin 1 used for room-temperature fatigue test.
- 20 May 1992* Sample 4\_30\_1 pin 1 used for retention after fatigue measurement. Sample 4\_30\_1 pin 16 used for retention measurement (nonfatigued). Sample 4\_30\_2 pin 2 used for high-temperature fatigue measurement.
- 21 May 1992* Sample 4\_30\_2 pin 2 used for high-temperature retention after fatigue measurement. Sample 4\_30\_1 pin 15 used for ionizing radiation test. Sample 121\_2\_1 (100 × 100 simple capacitor) used for ionizing radiation test.
- 22 May 1992* Sample 4\_30\_2 pin 2 used for retention measurement at room temperature after high-temperature stressing. Brad Melnick departs with all used and unused Y1 samples, both packaged and wafers.
- 28 May 1992* Initial report of test results to Jane Alexander of DARPA.

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